REMARKS

This Response responds to the Office Action dated June 24, 2009, in which the Examiner rejected claims 1-8, 10-19, and 21-22 under 35 U.S.C. § 103, and objected to claims 9 and 20 as being dependent upon a rejected based claim but would be allowable if rewritten in independent form.

Claim 1 claims an interleaving device and claim 12 claims an interleaving method. The device and method include a first interleaving means/step performing folding interleaving on first data comprised of plural input packets, in units of a data word or plural consecutive data words. A second interleaving means/step performs interleaving, in units of a packet, on second data directly output/generated by the first interleaving means/step. The second data is comprised of plural packets.

By performing interleaving on second data directly output/generated by a first interleaving means/step as claimed in claims 1 and 12, claimed invention provides an interleaving device and method which can correct a significant burst error using an error correction code having a small code length. The prior art does not show, teach or suggest the invention as claimed in claims 1 and 12.

Claims 1-8, 10-19 and 21-22 were rejected under 35 U.S.C. § 103 as being unpatentable over *Sako* (U.S. Patent No. 5,732,088) in view of *Higashida, et al.* (U.S. Patent No. 6,826,181) and further in view of *Weldon, Jr.* (U.S. Patent No. 5,140,596).

Applicant respectfully traverses the Examiner's rejection of the claims under 35 U.S.C. § 103. The claims have been reviewed in light of the Office Action, and for reasons which will be set forth below, Applicant respectfully requests the Examiner withdraws the rejection to the claims and allows the claims to issue.

Sako appears to disclose in FIG. 1 interleavers 3a or 3b change the data symbols or the code sequence of the parity generated by the C2 encoder (Col. 5, lines 17-19). The two interleavers 3a and 3b are provided for selecting the interleave length corresponding to the record density of the optical disk 20 (Col. 5, lines 60-62). The interleaver 3a is selected when the optical disk 20 is a standard record density type optical disk. The interleaver 3b is selected when the optical disk is a high density optical disk (Col. 6, lines 18-22). FIG. 6 shows an error-correction encoding process in which data is recorded on a standard density type optical disk. Input symbols are supplied to a C1 encoder 105. The output is supplied to a C2 encoder 102 through a delay circuit group 103a for the interleaving process. The C2 encoder 102 generates a C2 parity Q of 14 bytes with a Reed-Solomon Code. The C1 encoder 105 encodes not only data, but the C2 parity of the C1 code. Thus, the C2 parity Q is fed back from the C2 encoder 102 to the C1 encoder 105 through the delay circuit group 107a for the interleaving process. The delay circuit groups 103a and 107a compose the interleavers for the standard density type optical disk (Col. 9, lines 15-35).

Thus, *Sako* merely discloses in FIG. 1 interleavers 3a, 3b. However, the output from interleaver 3a in *Sako* is <u>not</u> directly input to interleaver 3b. Therefore, nothing in *Sako* shows, teaches or suggests a second interleaving means that directly receives output from a first interleaving means as claimed in claim 1, or a second interleaving step of performing interleaving on second data directly generated by a first interleaving step as claimed in claim 12. Rather, *Sako* teaches away from the claimed invention since the output from interleavers 3a, 3b are selectively output to C1 encoder 5.

Additionally, *Sako* merely discloses selecting interleaver 3a when an optical disk 20 is a standard record density and selecting interleaver 3b when the optical disk is a high density type optical disk. Thus, nothing in *Sako* shows, teaches or suggests a first interleaving means performing interleaving in units of a data word or plural consecutive data words, and second interleaving means performing interleaving in units of a packet as claimed in claims 1 and 12. Rather, *Sako* merely discloses using interleaver 3a when the optical disk is a standard record density and selecting interleaver 3b when the optical disk is a high density optical disk.

Higashida, et al. appears to disclose in FIGS. 21, 26, 29 and 36, a first interleaving processing means for executing a first interleaving process by writing a data string into a first storage apparatus having a first matrix form in a first direction and thereafter reading from the first storage apparatus the data in a second direction perpendicular to the first direction and outputting the data after the first interleave process in a unit of data in the second direction. A second parity adding means adds a predetermined parity to data output from the first interleave processing means and outputs the data. A second interleave processing means executes a second interleave process by writing the data output from the second parity adding means into a second storage apparatus having a second matrix form in a fourth direction of the second matrix coinciding with the second direction of the first matrix and thereafter reading from the second storage apparatus the data in a third direction perpendicular to the fourth direction of the second matrix and outputting the data obtained after the second interleave process in a unit of data in the third direction (Col. 4, lines 24-55).

Thus, *Higashida, et al.* merely discloses a second interleave processing means executing a second interleave process on data output from a parity adding means. Nothing in *Higashida, et al.* shows, teaches or suggests (a) a second interleaving means directly receiving output from a first interleaving means as claimed in claim 1, or (b) a second interleaving step of performing interleaving on second data directly generated by a first interleaving step as claimed in claim 12. Rather, *Higashida, et al.* merely discloses that the second interleaving means executes an interleave process on data output from a parity adding means.

Furthermore, *Higashida, et al.* merely discloses that the data output from the second interleaving means is output in a unit of data in a third direction. Thus, nothing in *Higashida, et al.* shows, teaches or suggests (a) a first interleaving in units of a data word or plural consecutive data words, and (b) second interleaving in units of a packet as claimed in claims 1 and 12. Rather, *Higashida, et al.* merely discloses after a first interleave process outputting data of a unit of a second direction and after a second interleave process outputting data of a unit of data in a third direction.

Weldon, Jr. appears to disclose in FIG. 3 a serial interleaving and encoding system (Col. 8, lines 9-10). The system includes a first serial interleaver 300 which interleaves incoming user data (Col. 8, lines 13-14). The serial interleaver 300 receives and outputs data one byte at a time (Col. 8, lines 18-19). The serial interleaver 300 transmits at its output 300b block of 24 interleaved bytes at a time (Col. 8, lines 25-28). A serial encoder 310 produces the parity check characters. The serial encoder 310 receives from the serial interleaver 300 a block of 24 interleaved bytes one byte at a time, and passes the bytes along at its output 310a to a second serial interleaver 320. It then

transmits the 4 parity check characters at its output 310a (Col. 8, lines 34-42). The second serial interleaver 320 interleaves the 28-byte code words received from the outer serial encoder 310 (Col. 8, lines 46-48). The serial interleaver 320 receives and outputs data one byte at a time (Col. 8, lines 51-52).

Thus, *Weldon, Jr.* merely discloses that the serial interleaver 320 outputs data to serial encoder 310 and the serial encoder 310 outputs data to the second interleaver 320. Thus, nothing in *Weldon, Jr.* shows, teaches or suggests (a) a second interleaving means directly reeeiving output from a first interleaving means as a claimed in claim 1, or (b) a second interleaving step of performing interleaving on second data directly generated by a first interleaving step as claimed in claim 12. Rather, *Weldon, Jr.* teaches away from the claimed invention since the first interleaver outputs to serial encoder 310 and not to the serial interleaver 320.

Furthermore, *Weldon, Jr.* clearly discloses that both the first and second serial interleavers 300 and 320 output data one byte at a time. Nothing in *Weldon, Jr.* shows, teaches or suggests (a) a first interleaving means performing folding interleaving in units of a data word or plural consecutive data words, and (b) a second interleaving means interleaving in units of a packet as claimed in claims 1 and 12. Rather, *Weldon, Jr.* only discloses that the interleavers 300, 320 output data one byte at a time.

The combination of *Sako*, *Higashida, et al.*, and *Weldon, Jr.* would not be possible since the interleavers 3a and 3b of *Sako* separately output data to an encoder whereas *Higashida, et al.* and *Weldon, Jr.* output interleaved data to an intermediate circuit (parity adding circuit in *Higashida, et al.* or serial encoder 310 of *Weldon, Jr.*). Even assuming arguendo that the references could be combined, the combination would

merely suggest that after selecting an output from interleavers 3a or 3b, to output the selected interleaved data to an intermediate circuit such as the parity adding circuit as taught by *Higashida, et al.*, or the serial encoder 310 as taught by *Weldon, Jr.* Thus, nothing in the combination of the references shows, teaches or suggests (a) a first interleave mean performing folding interleaving in units of a data word or plural consecutive data words and a second interleaving means directly receiving output from the first interleave means and performing interleaving in units of a packet as claimed in claim 1, or (b) a first interleaving step of performing folding interleave in units of a data word or plural consecutive data words and a second interleaving step of performing interleaving in units of a packet of second data directly generated by the first interleaving step as claimed in claim 12. Therefore, Applicant respectfully requests the Examiner withdraws the rejection to claims 1 and 12 under 35 U.S.C. § 103.

Claims 2-8, 10-11, 13-19 and 21-22 depend from claims 1 and 12 and recite additional features. Applicant respectfully submits that claims 2-8, 10-11, 13-19 and 21-22 would not have been obvious within the meaning of 35 U.S.C. § 103 over *Sako*, *Higashida, et al.* and *Weldon, Jr.*, at least for the reasons as set forth above. Therefore, Applicant respectfully requests the Examiner withdraws the rejection to claims 2-8, 10-11, 13-19 and 21-22 under 35 U.S.C. § 103.

Since objected to claims 9 and 20 depend from allowable claims, Applicant respectfully requests the Examiner withdraws the objection thereto.

Thus it now appears that the application is in condition for a reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested.

CONCLUSION

If for any reason the Examiner feels that the application is not now in condition for allowance, the Examiner is requested to contact, by telephone, the Applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, Applicant respectfully petitions for an appropriate extension of time. The fees for such extension of time may be charged to Deposit Account No. 50-0320.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 50-0320.

Respectfully submitted,

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